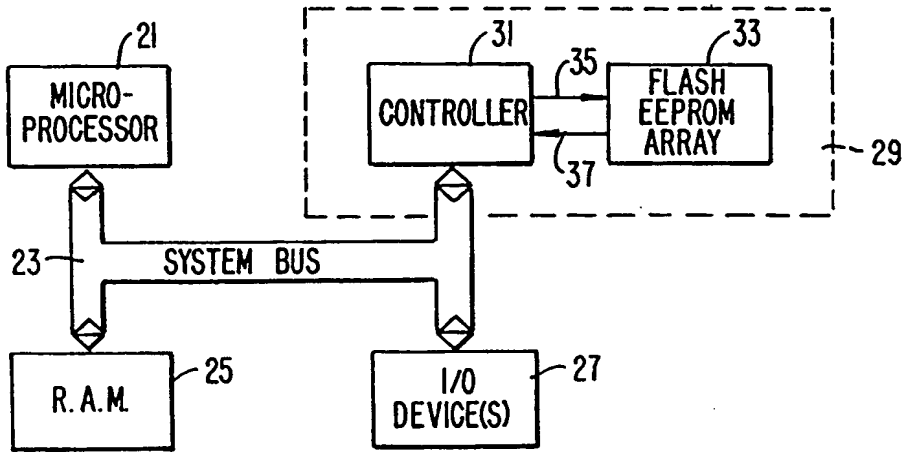

21
MICRO-
PROCESSOR
31
CONTROLLER
35
33
FLASH
EEPROM
ARRAY
37
29
23
SYSTEM BUS
R.A.M.
25
I/O
DEVICE(S)
27

FIG._1A

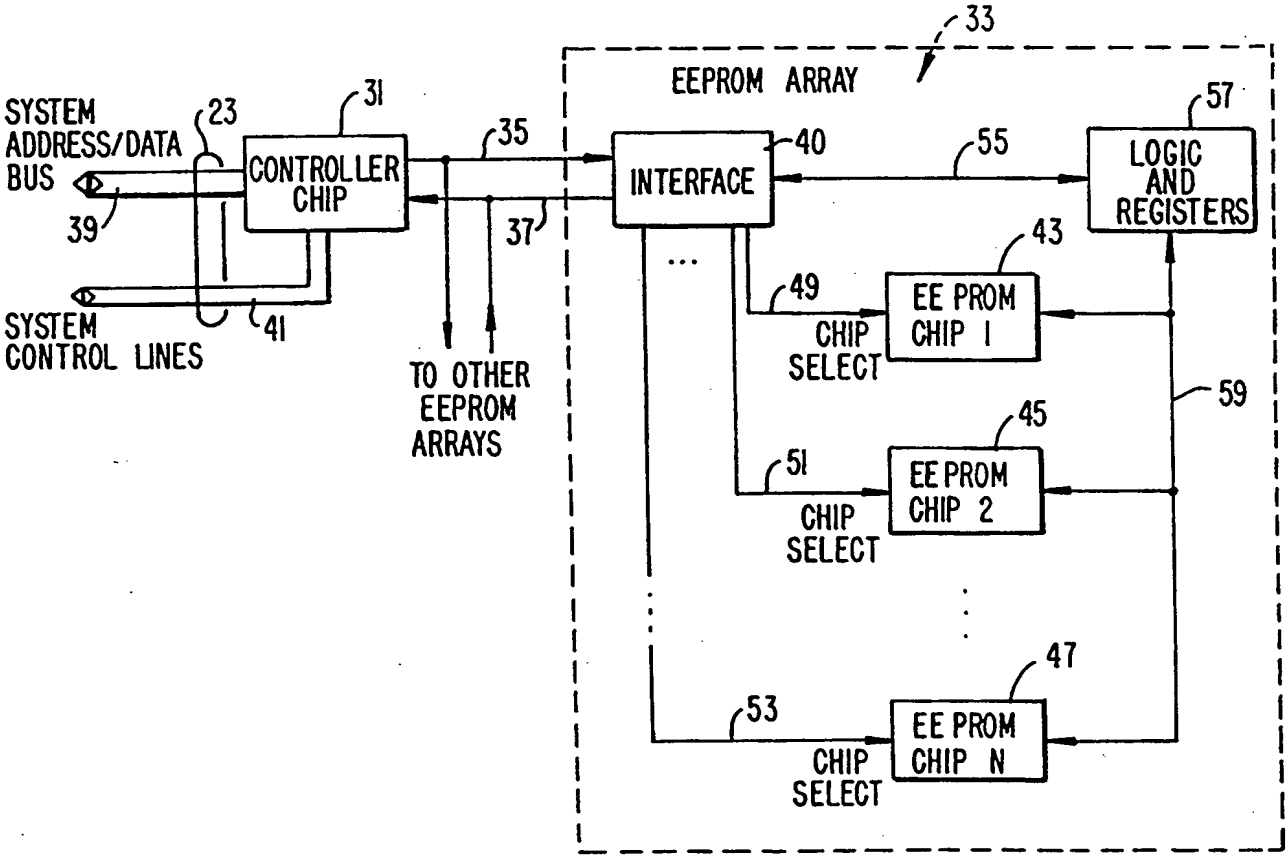

33
EEPROM ARRAY
SYSTEM
ADDRESS/DATA
BUS
23
31
CONTROLLER
CHIP
35
39
37
SYSTEM
CONTROL LINES
41
TO OTHER
EEPROM
ARRAYS
INTERFACE
40
55
57
LOGIC
AND
REGISTERS
43
49
EE PROM
CHIP 1
CHIP
SELECT
59
45
51
EE PROM
CHIP 2
CHIP
SELECT
47
53
EE PROM
CHIP N
CHIP
SELECT

FIG._1B

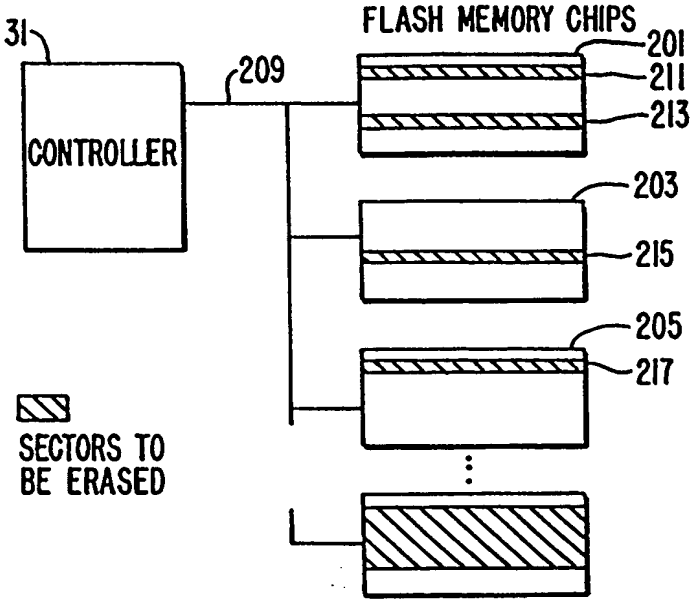


FIG._2

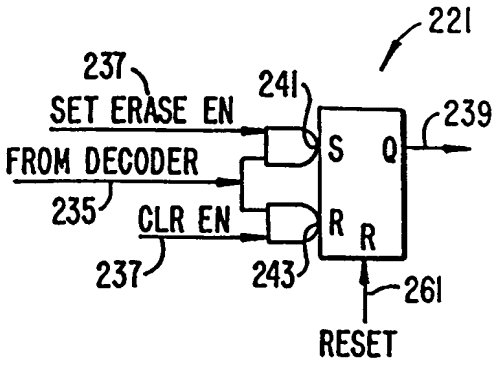


FIG._3B

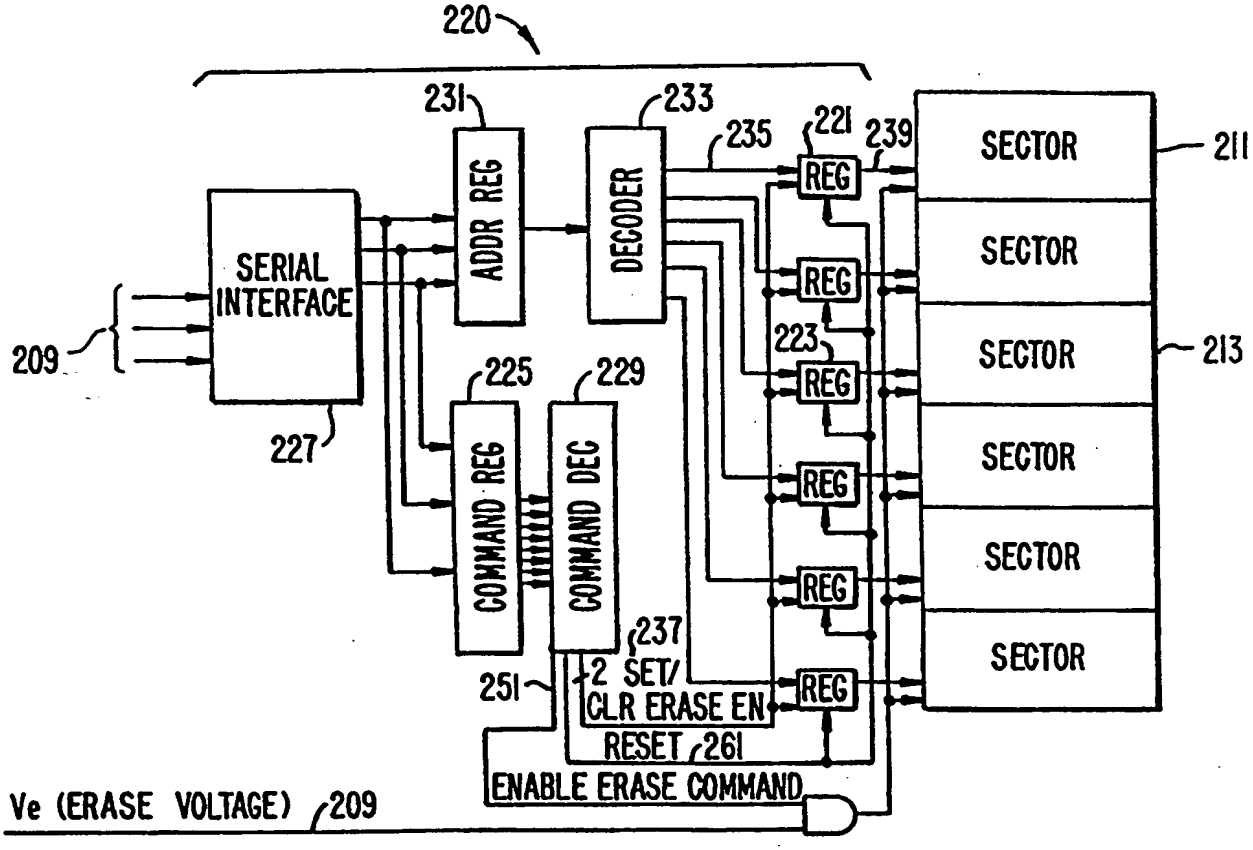


FIG._3A

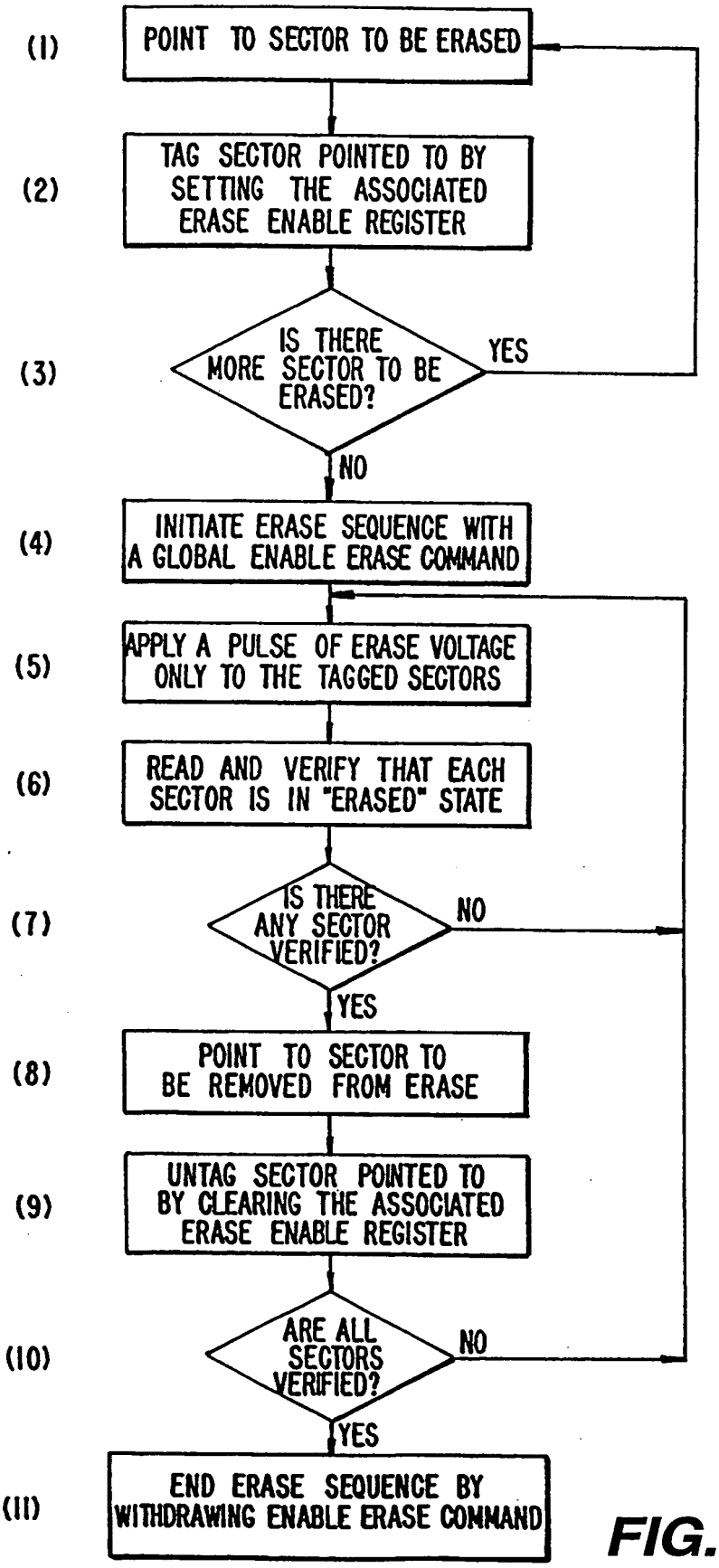


FIG._4

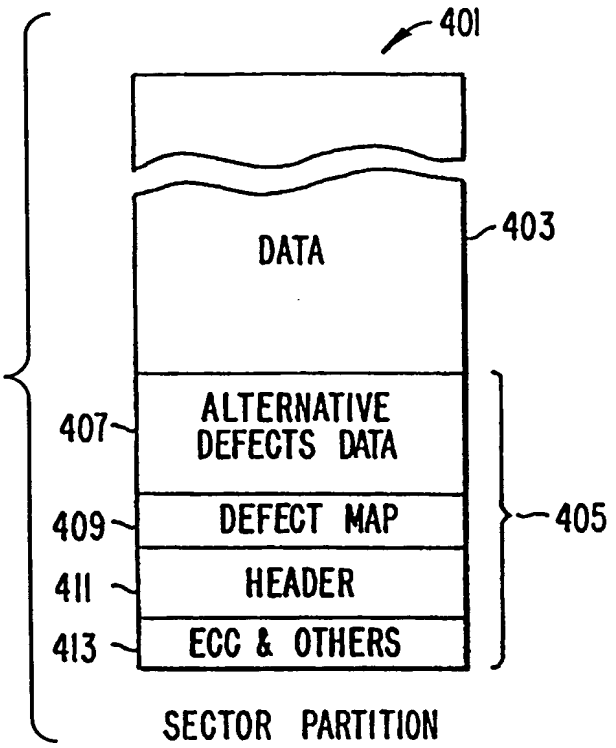
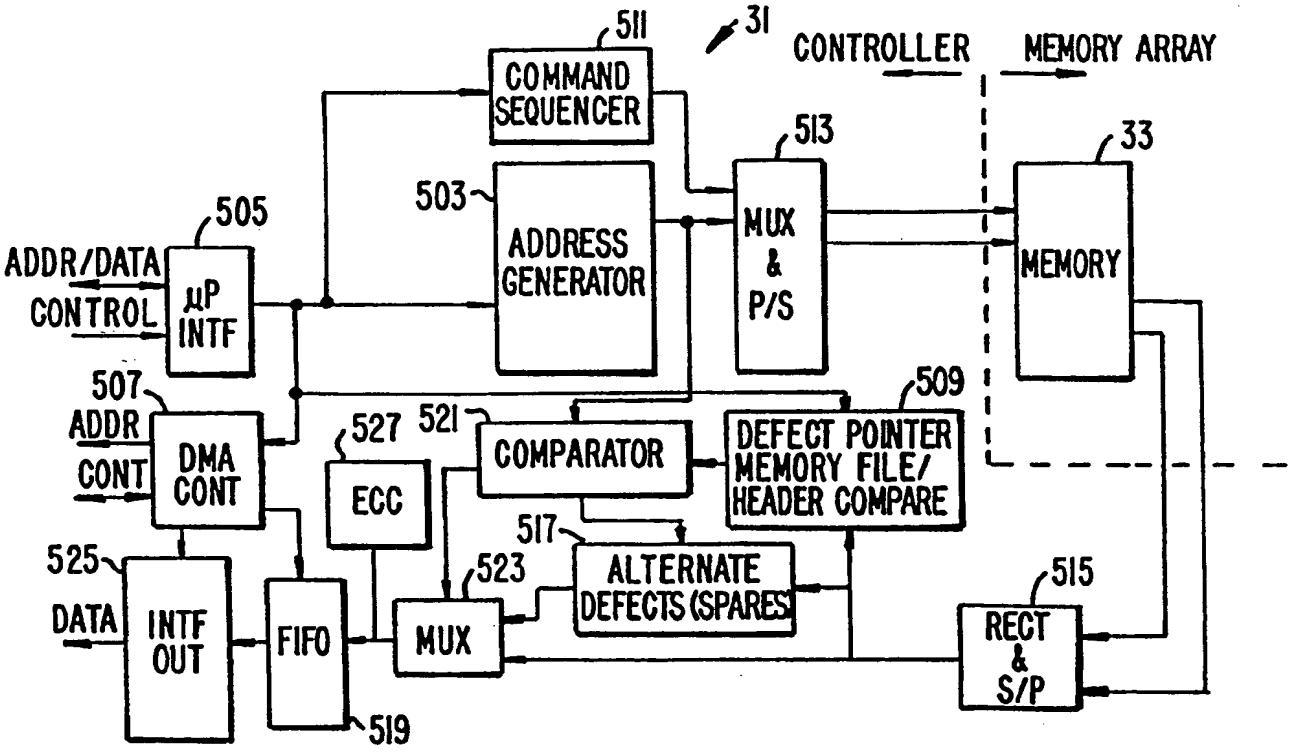
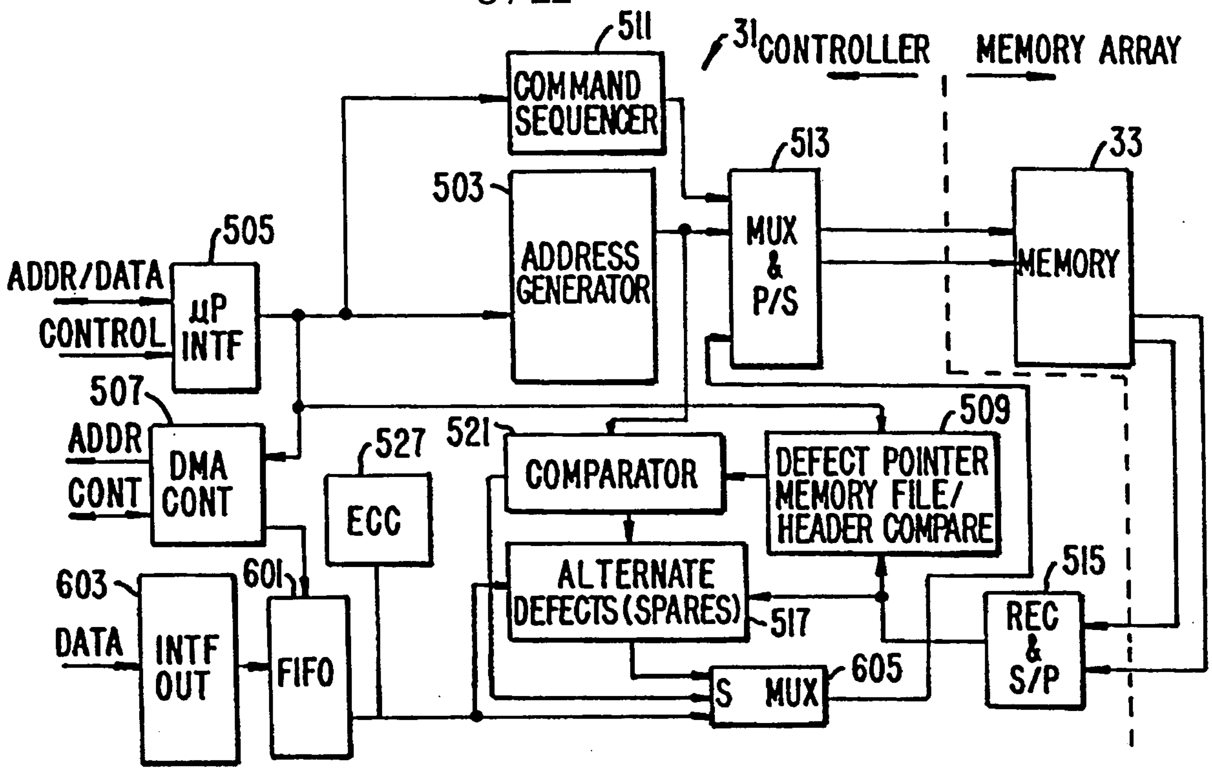


FIG._5



READ DATA PATH CONTROL

FIG._6



WRITE DATA PATH CONTROL

FIG._7

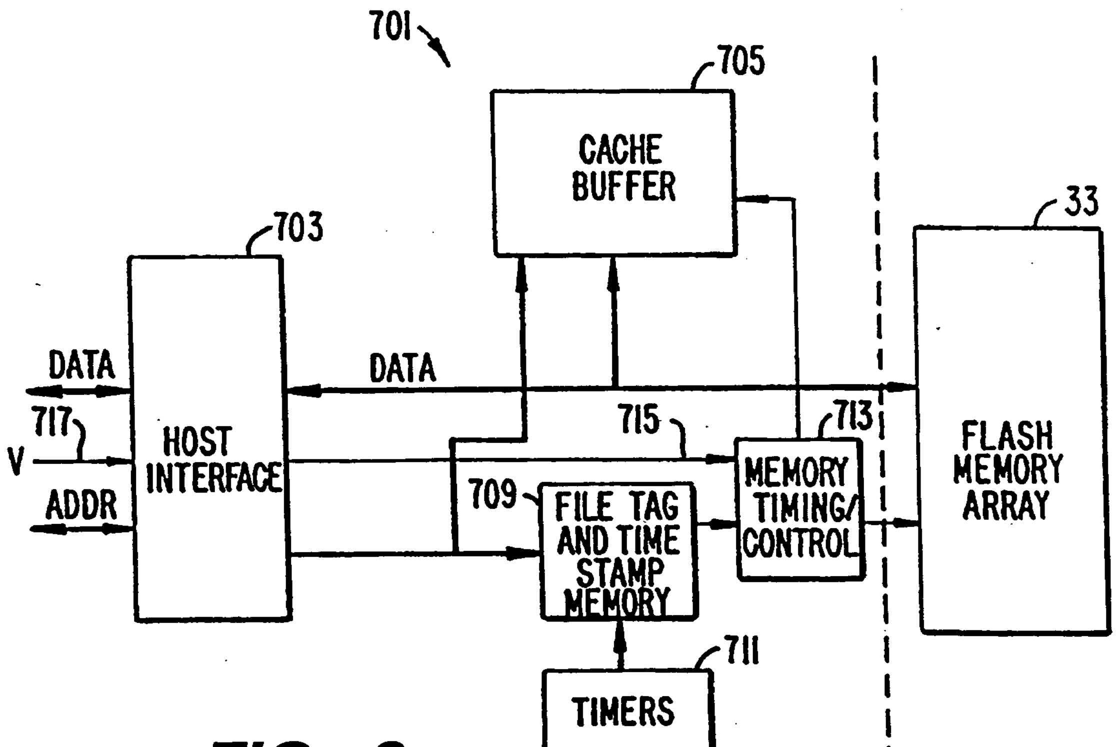


FIG._8

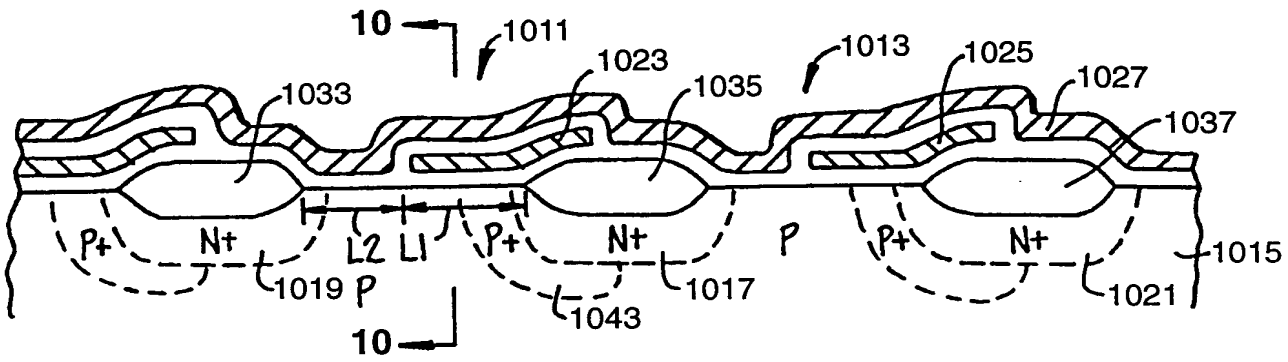


FIG._9

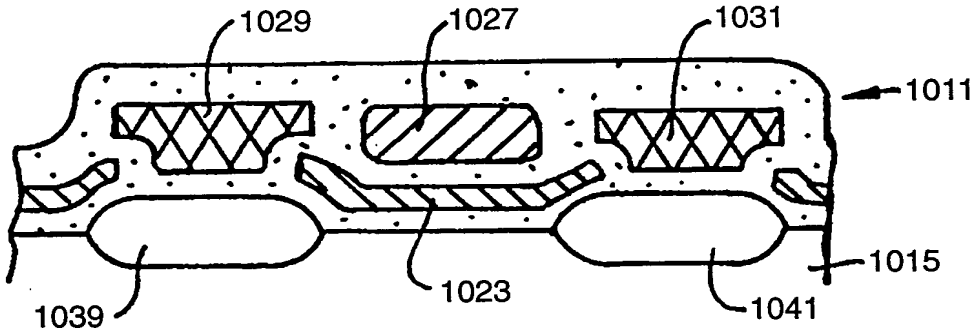


FIG._10

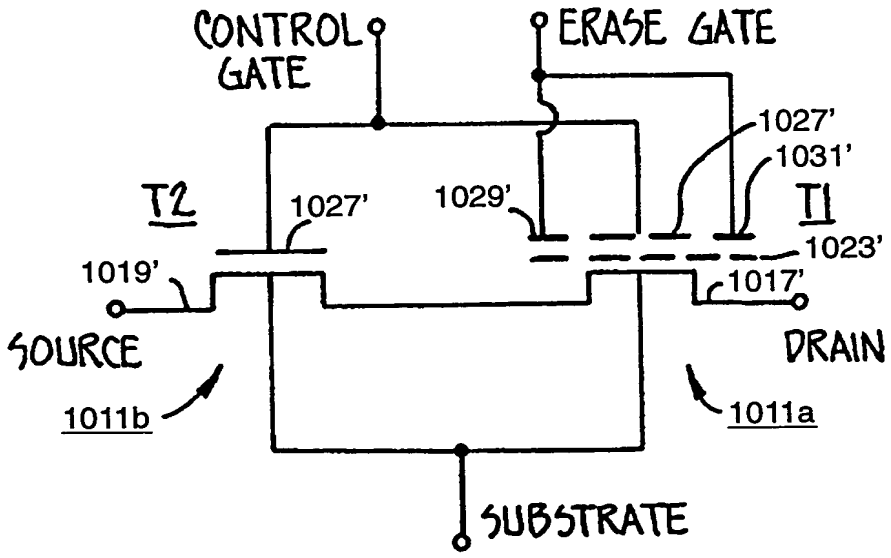


FIG._11

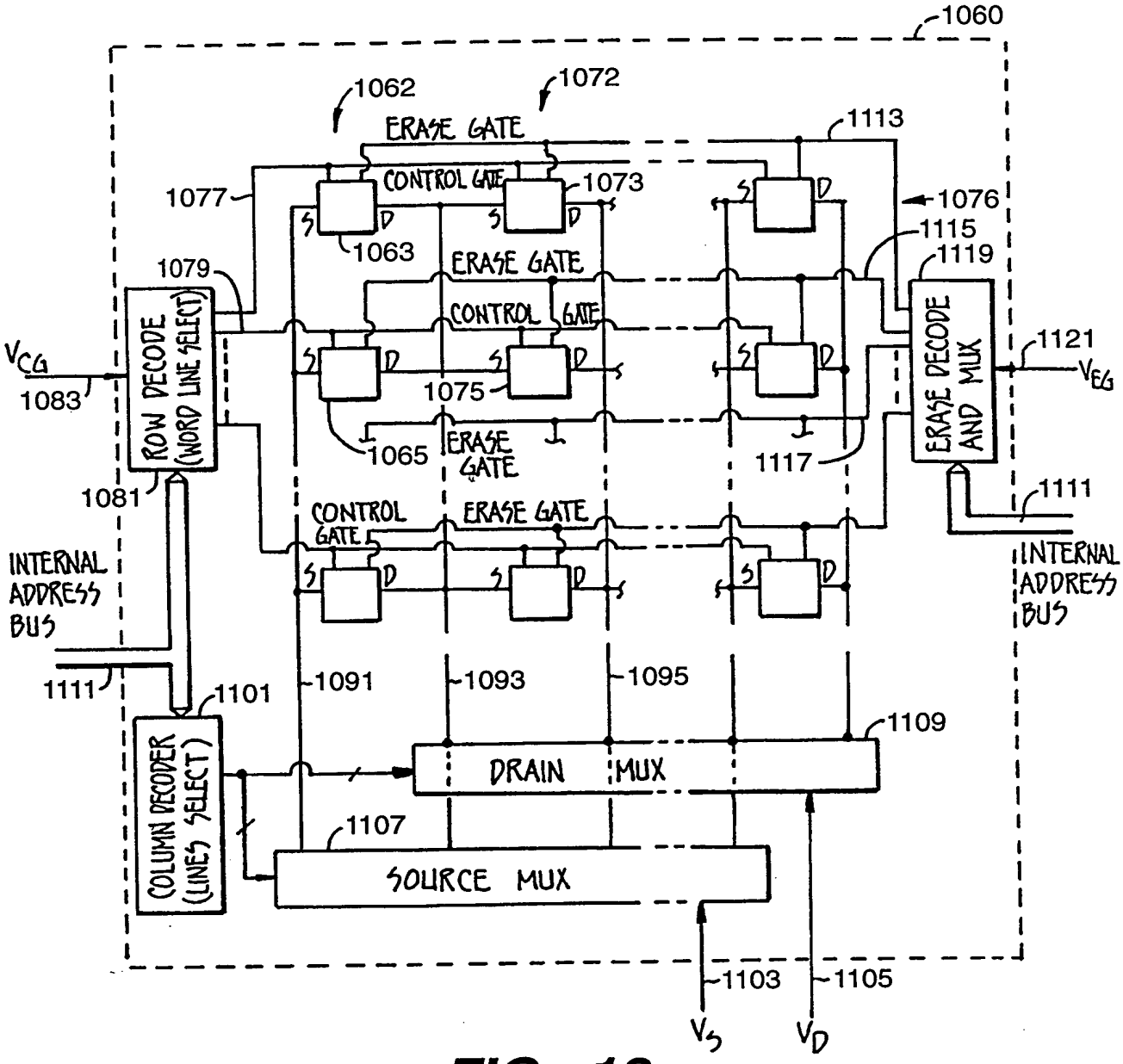

1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
1115
1119
ERASE GATE
1079
CONTROL GATE
ROW DECODE (WORD LINE SELECT)
ERASE DECODE AND MUX
1121
V_{CG}
1083
1075
V_{EG}
1065
ERASE GATE
1117
1081
1111
CONTROL GATE
ERASE GATE
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1091
1093
1095
1101
1109
COLUMN DECODER (LINES SELECT)
DRAIN MUX
1107
SOURCE MUX
1103
1105
V_S
V_D

FIG._12

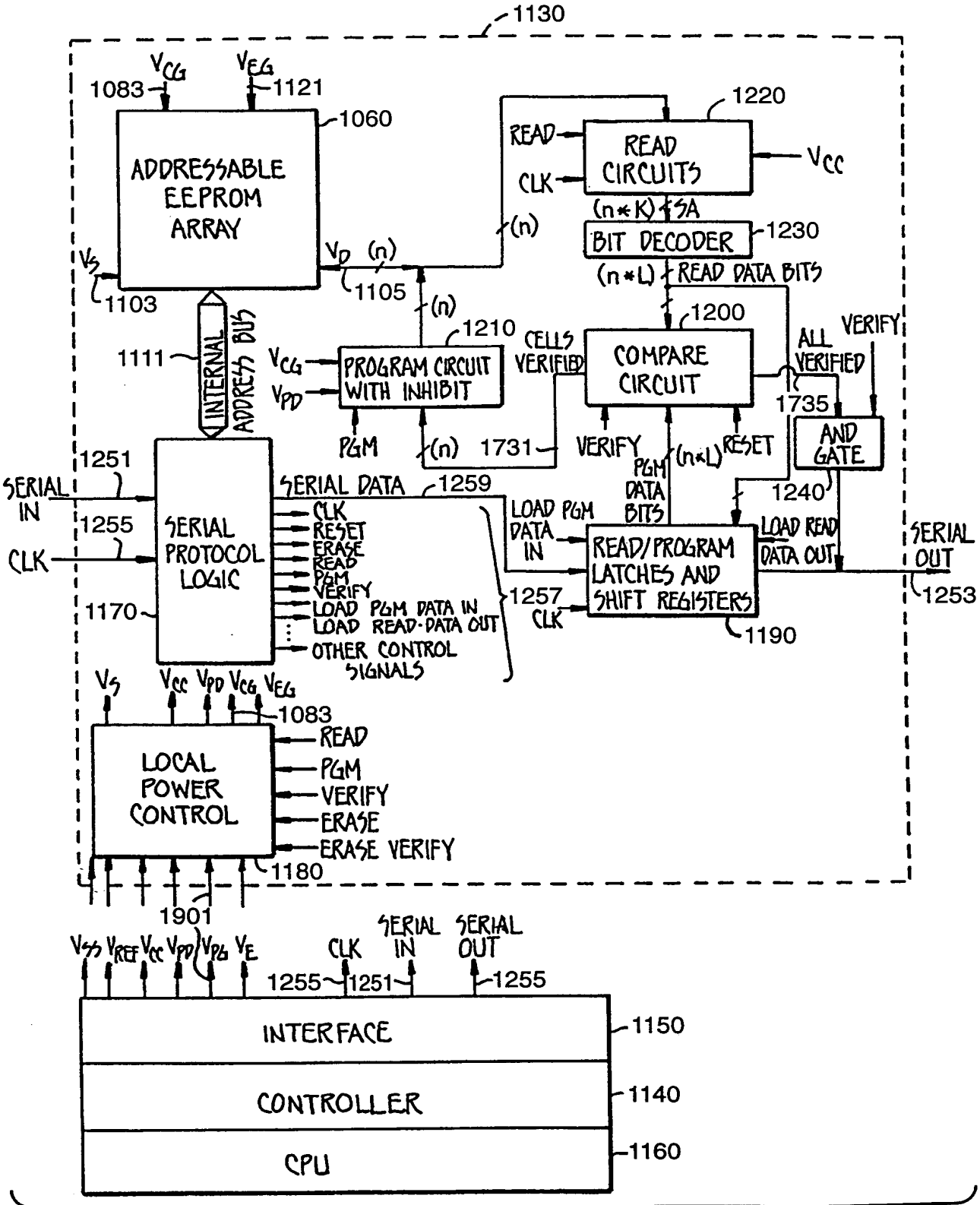

1130
V_{CG}
V_{EG}
1083
1121
1060
ADDRESSABLE EEPROM ARRAY
V_S
1103
V_D (n)
1105
1111
INTERNAL ADDRESS BUS
1210
V_{CG}
V_{PD}
PROGRAM CIRCUIT WITH INHIBIT
PGM
(n)
1731
READ
CLK
1220
READ CIRCUITS
V_{CC}
(n*K) SA
BIT DECODER
1230
(n*L) READ DATA BITS
1200
CELLS VERIFIED
COMPARE CIRCUIT
ALL VERIFIED
1735
VERIFY
AND GATE
1240
VERIFY
PGM DATA BITS
(n*L)
RESET
1251
SERIAL IN
1255
CLK
SERIAL PROTOCOL LOGIC
1170
SERIAL DATA
1259
CLK
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ DATA OUT
OTHER CONTROL SIGNALS
LOAD PGM DATA IN
1257
CLK
READ/PROGRAM LATCHES AND SHIFT REGISTERS
1190
LOAD READ DATA OUT
SERIAL OUT
1253
V_S
V_{CC}
V_{PD}
V_{CG}
V_{EG}
1083
LOCAL POWER CONTROL
READ
PGM
VERIFY
ERASE
ERASE VERIFY
1180
1901
V_{SS}
V_{REF}
V_{CC}
V_{PD}
V_{PG}
V_E
CLK
SERIAL IN
SERIAL OUT
1255
1251
1255
INTERFACE
1150
CONTROLLER
1140
CPU
1160

FIG._13

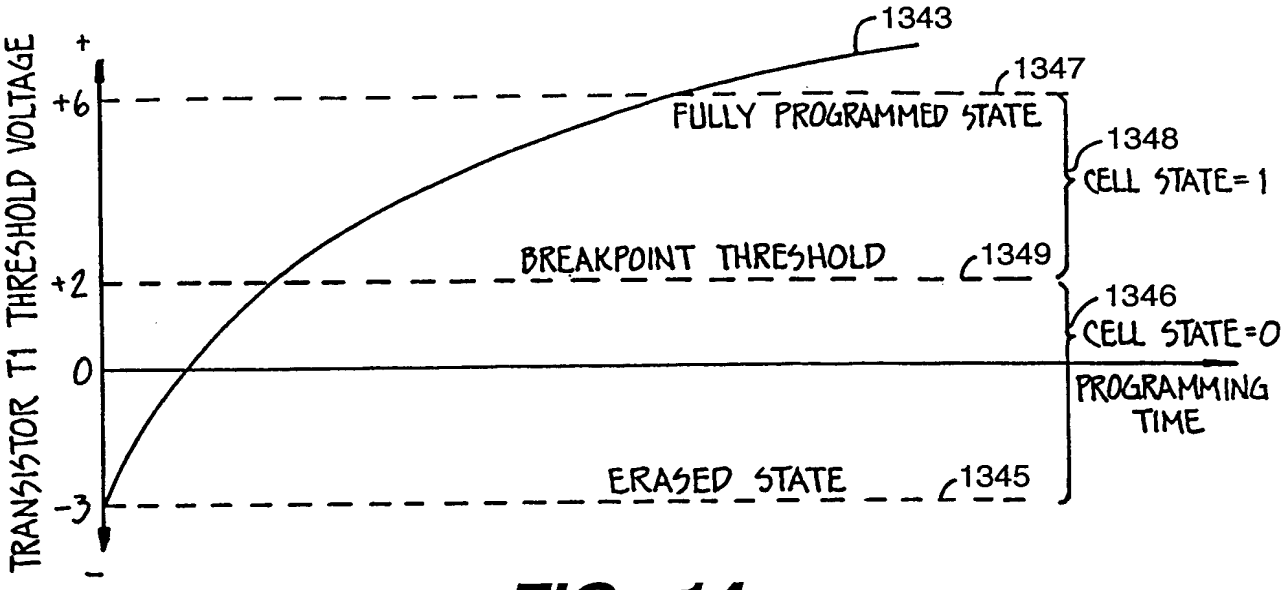


FIG._14

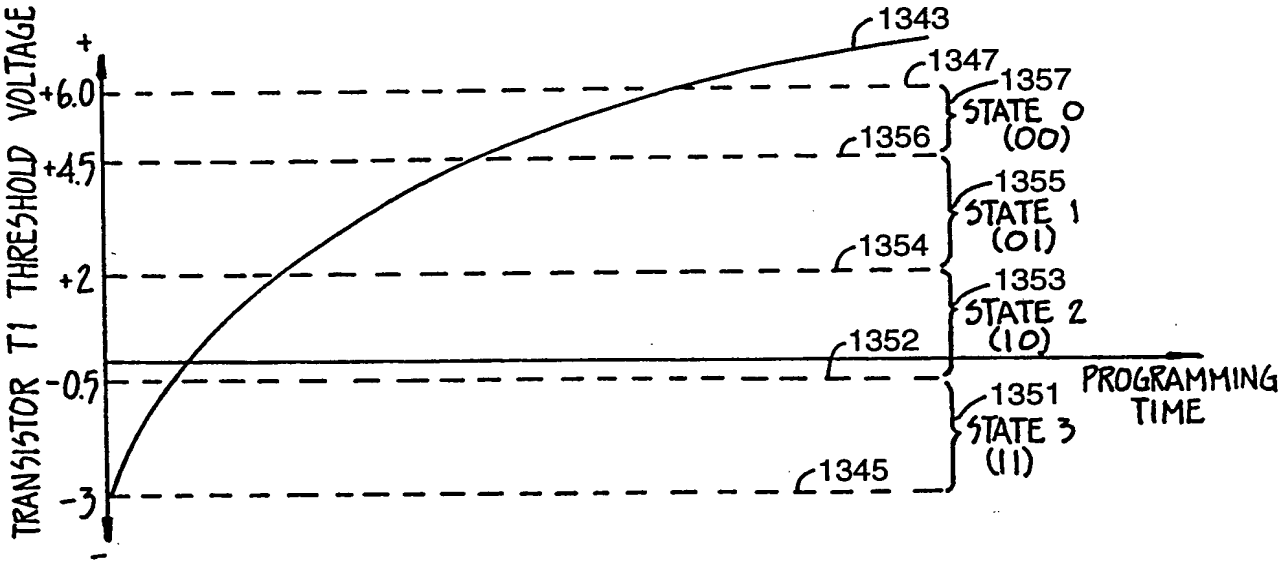


FIG._15A

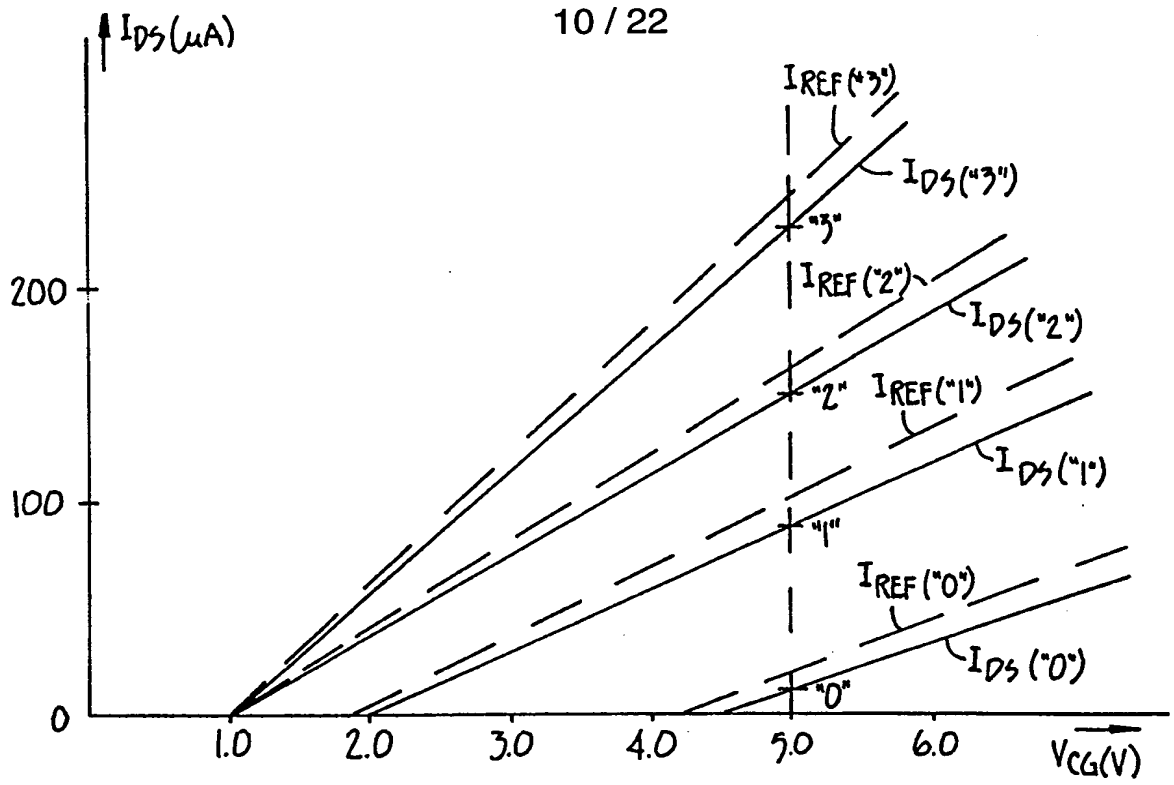


FIG._15B

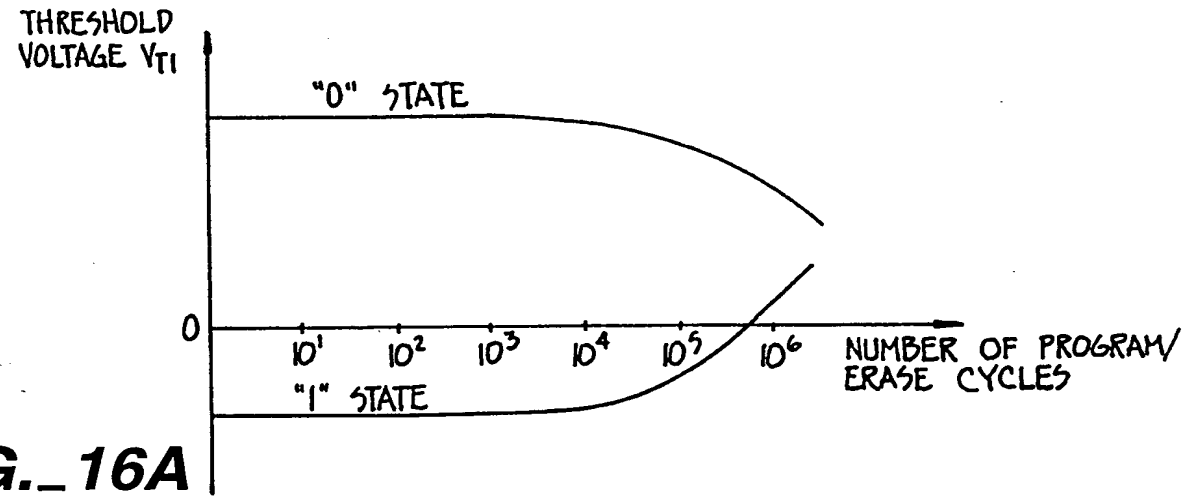


FIG._16A

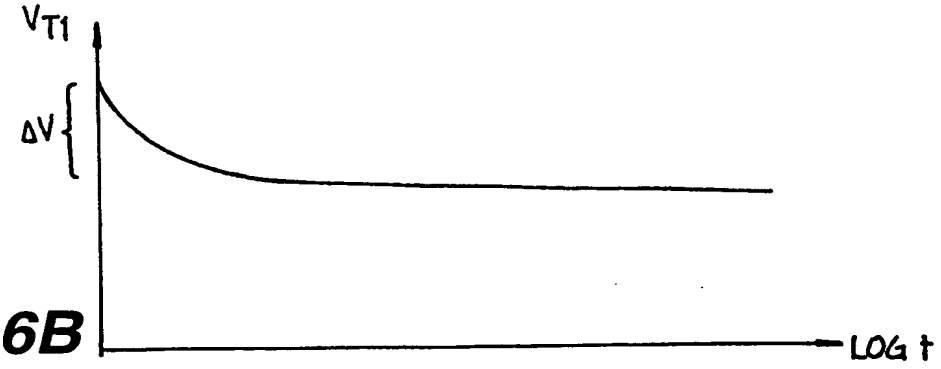


FIG._16B

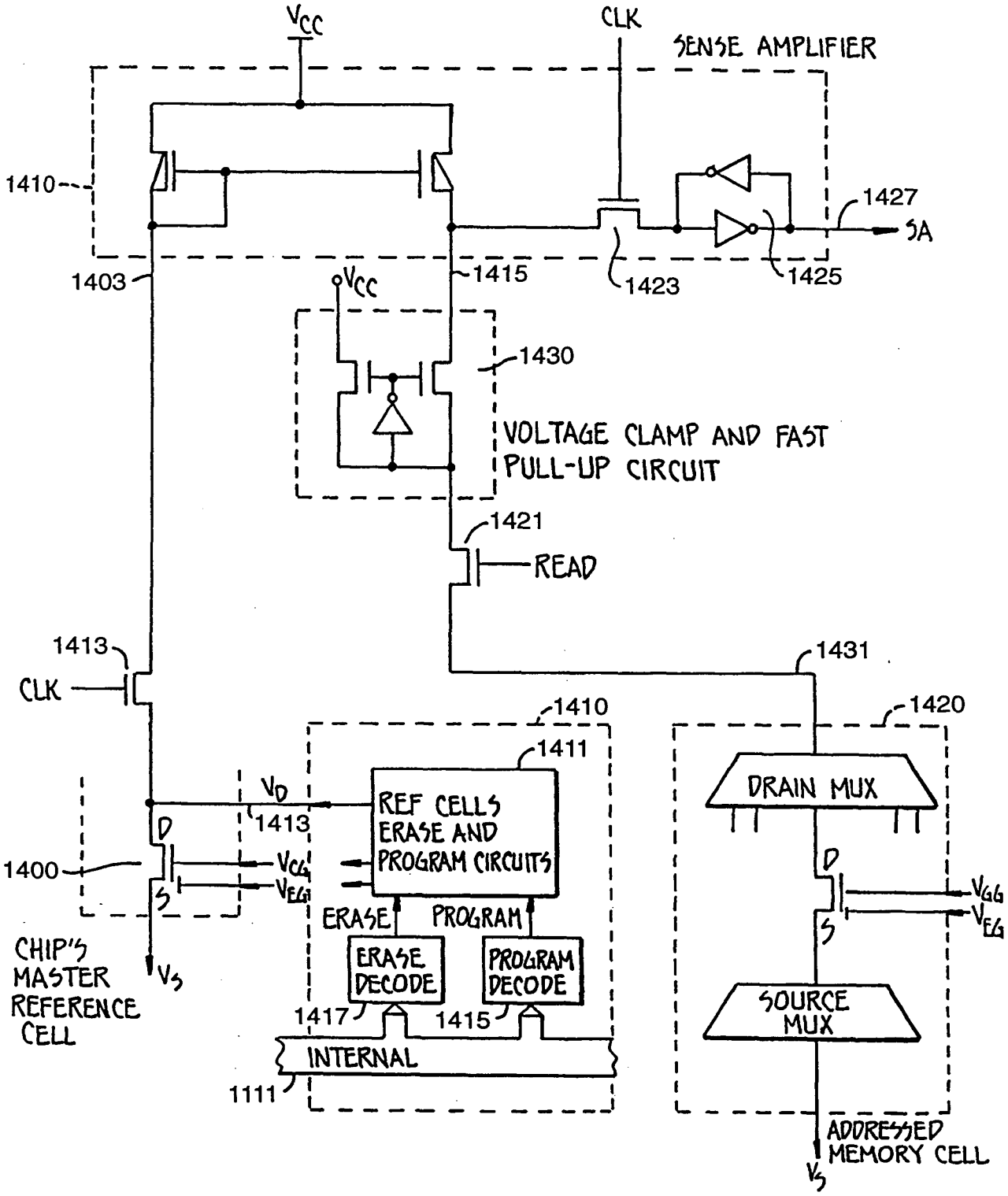

V_{CC}
CLK
SENSE AMPLIFIER
1410
1427
SA
1403
1415
1423
1425
V_{CC}
1430
VOLTAGE CLAMP AND FAST PULL-UP CIRCUIT
1421
READ
1413
CLK
1431
1410
1420
1411
V_D
1413
REF CELLS ERASE AND PROGRAM CIRCUITS
DRAIN MUX
D
1400
V_{GG}
V_{EG}
S
ERASE
PROGRAM
CHIP'S MASTER REFERENCE CELL
V_S
ERASE DECODE
PROGRAM DECODE
SOURCE MUX
1417
1415
INTERNAL
1111
ADDRESSED MEMORY CELL
V_S

FIG._17A

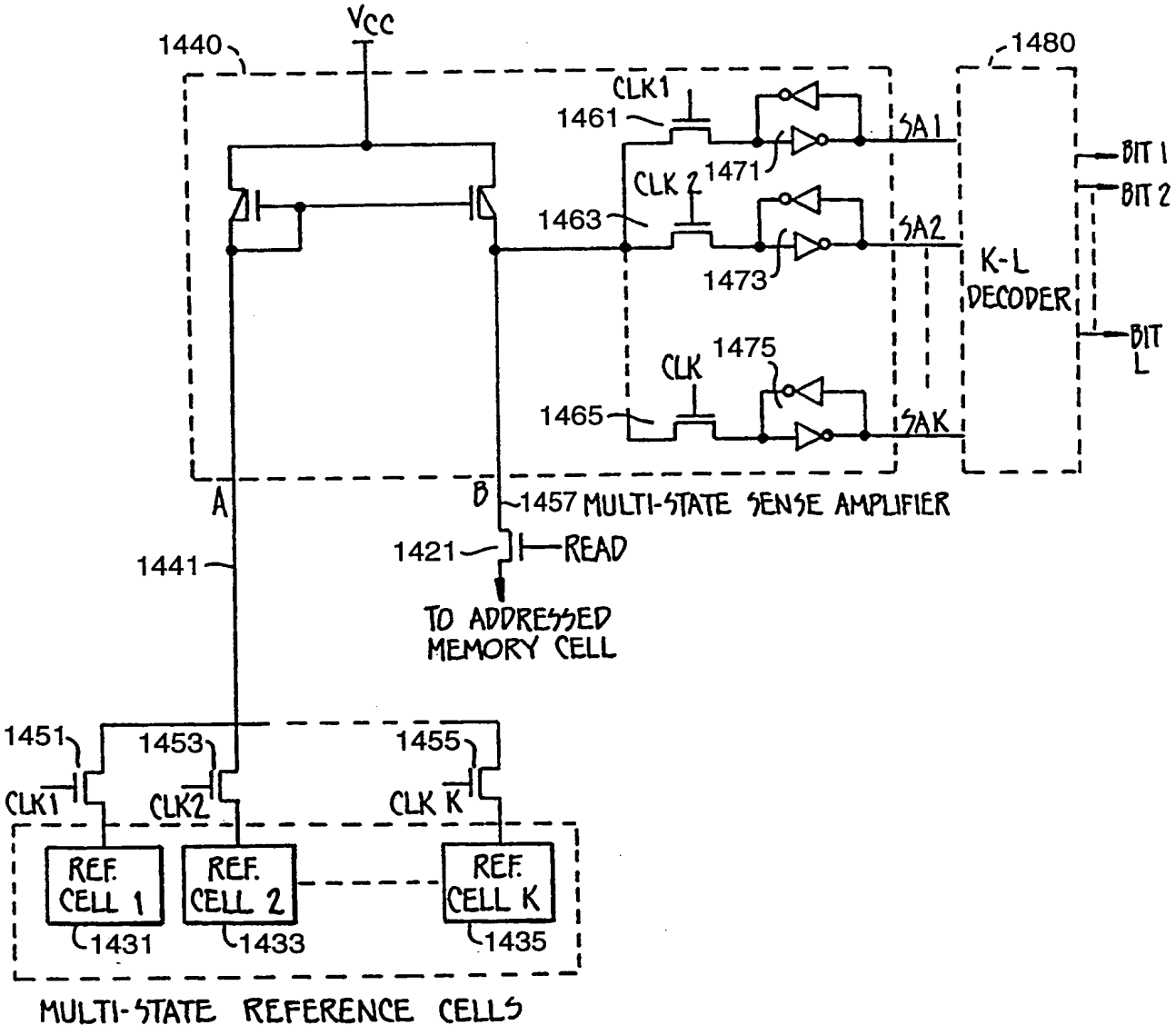

Vcc
1440
1480
CLK1
1461
SA1
1471
BIT 1
BIT 2
CLK 2
1463
SA2
1473
K-L
DECODER
BIT
L
CLK
1475
1465
SAK
A
B
1457 MULTI-STATE SENSE AMPLIFIER
1421
READ
1441
TO ADDRESSED
MEMORY CELL
1451
1453
1455
CLK1
CLK2
CLK K
REF.
CELL 1
REF.
CELL 2
REF.
CELL K
1431
1433
1435
MULTI-STATE REFERENCE CELLS

FIG._17B

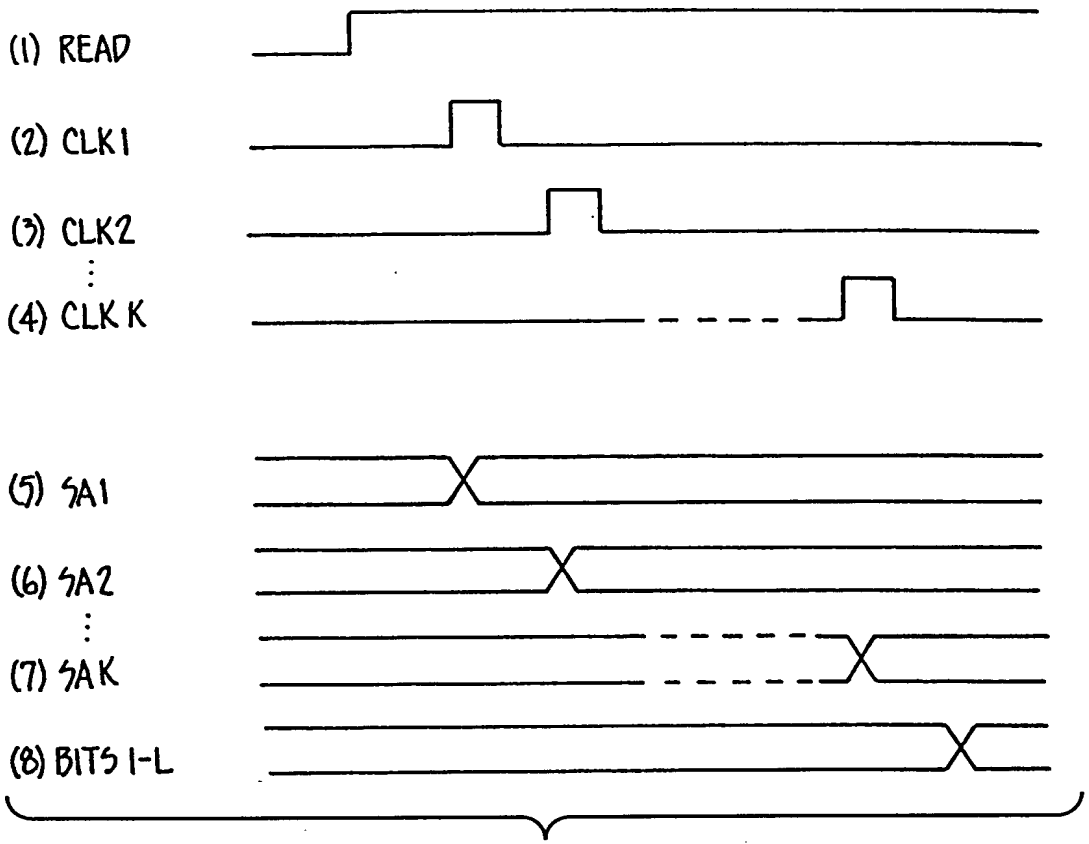


FIG._17C

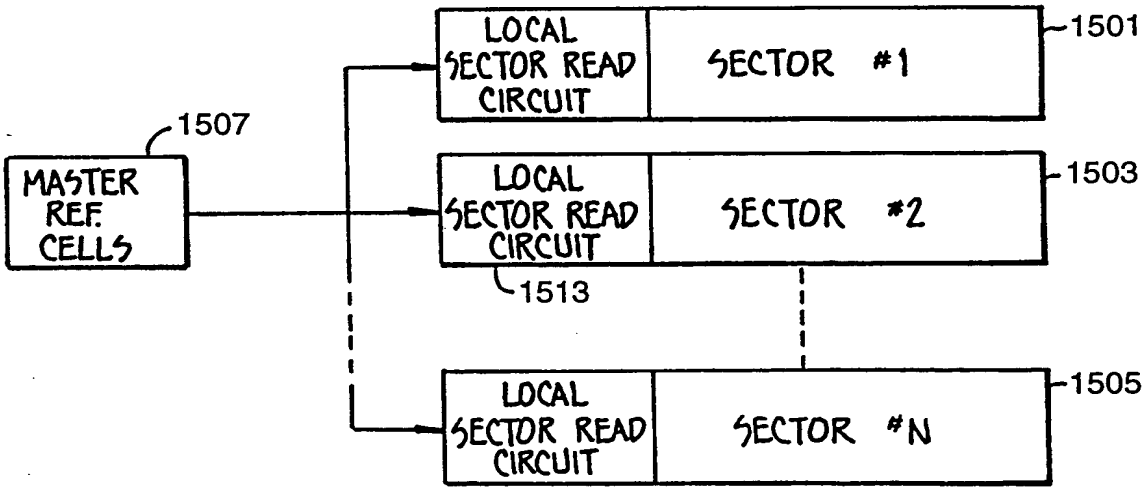


FIG._18

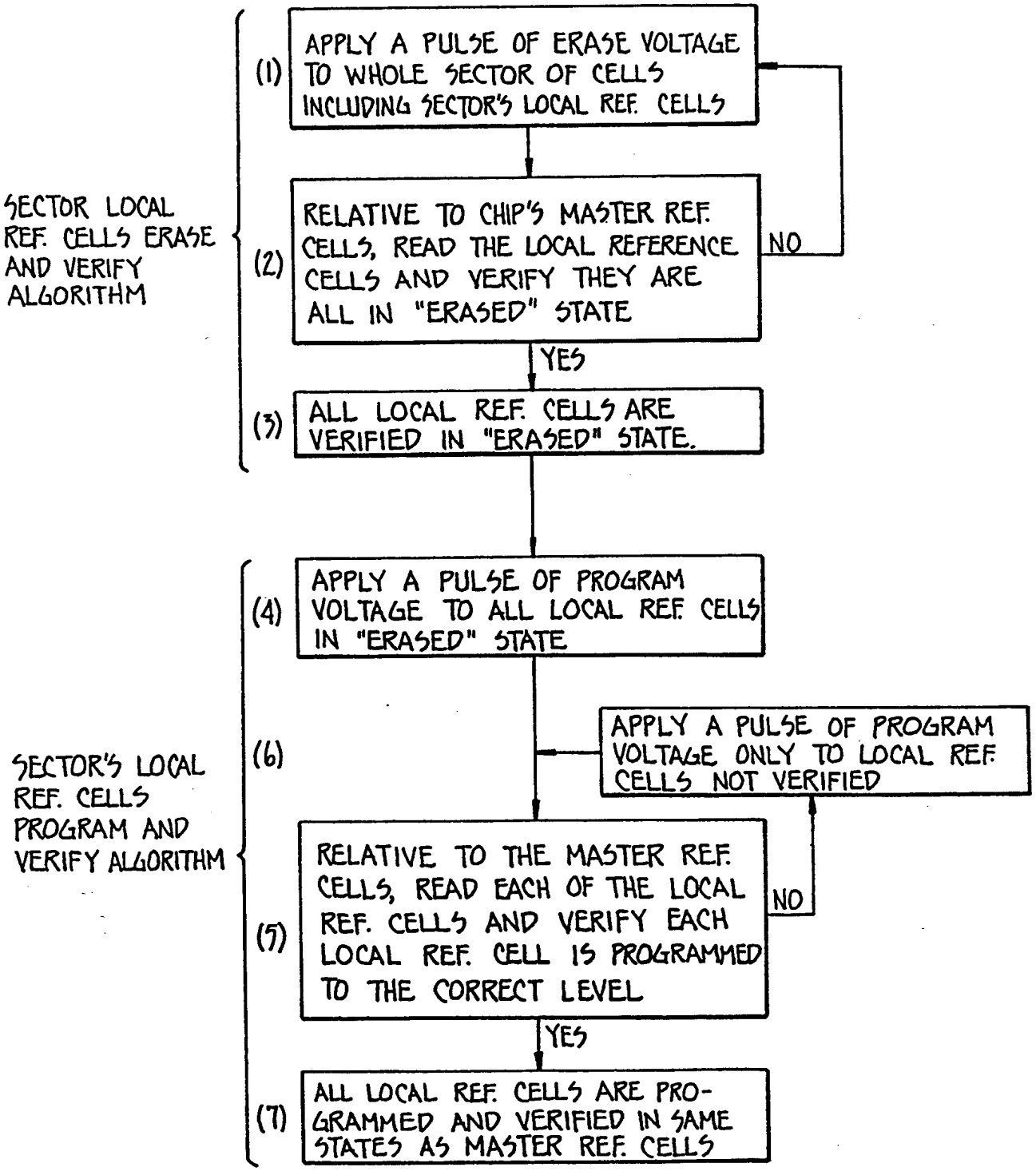

SECTOR LOCAL REF. CELLS ERASE AND VERIFY ALGORITHM
(1) APPLY A PULSE OF ERASE VOLTAGE TO WHOLE SECTOR OF CELLS INCLUDING SECTOR'S LOCAL REF. CELLS
(2) RELATIVE TO CHIP'S MASTER REF. CELLS, READ THE LOCAL REFERENCE CELLS AND VERIFY THEY ARE ALL IN "ERASED" STATE
NO
YES
(3) ALL LOCAL REF. CELLS ARE VERIFIED IN "ERASED" STATE.
SECTOR'S LOCAL REF. CELLS PROGRAM AND VERIFY ALGORITHM
(4) APPLY A PULSE OF PROGRAM VOLTAGE TO ALL LOCAL REF. CELLS IN "ERASED" STATE
(6) APPLY A PULSE OF PROGRAM VOLTAGE ONLY TO LOCAL REF. CELLS NOT VERIFIED
(5) RELATIVE TO THE MASTER REF. CELLS, READ EACH OF THE LOCAL REF. CELLS AND VERIFY EACH LOCAL REF. CELL IS PROGRAMMED TO THE CORRECT LEVEL
NO
YES
(7) ALL LOCAL REF. CELLS ARE PROGRAMMED AND VERIFIED IN SAME STATES AS MASTER REF. CELLS

FIG._19

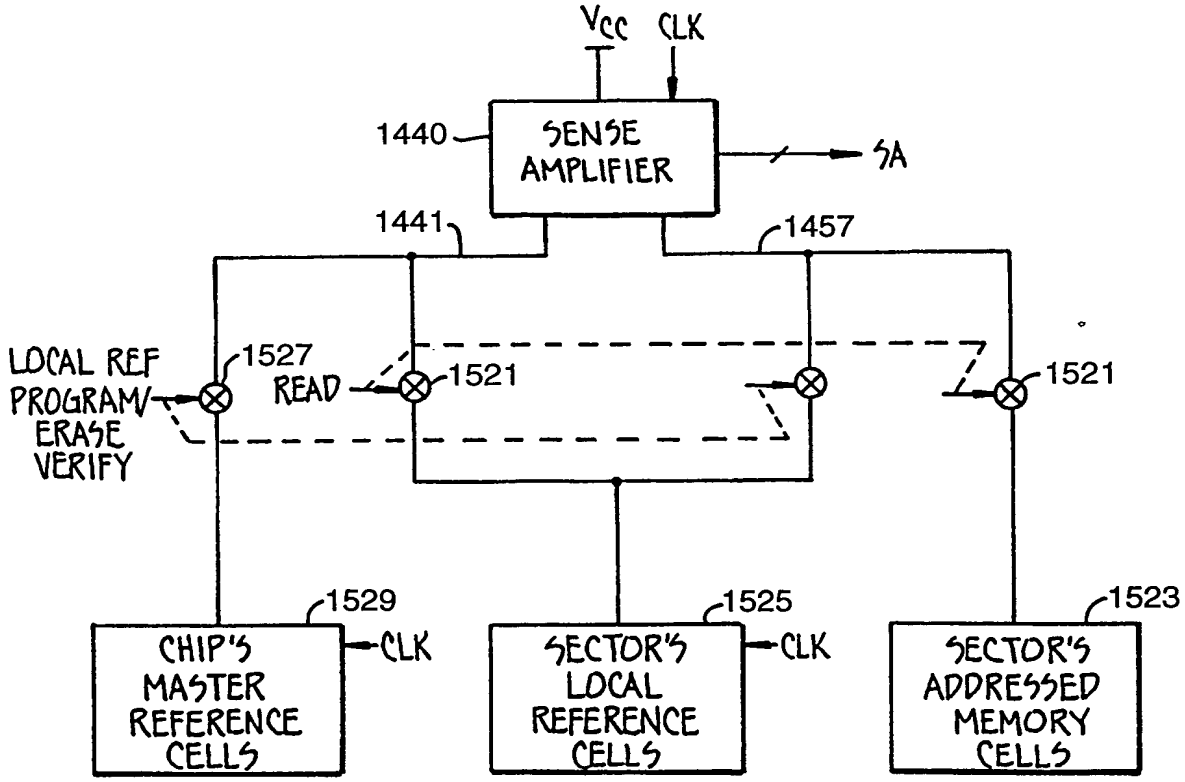


FIG._20A

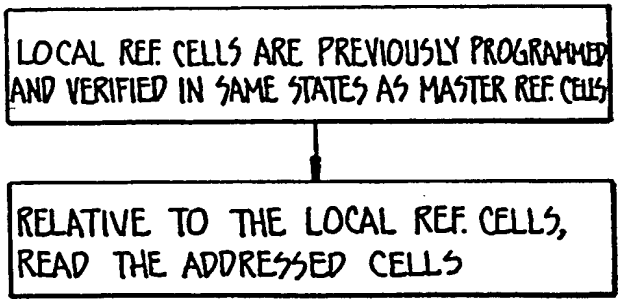
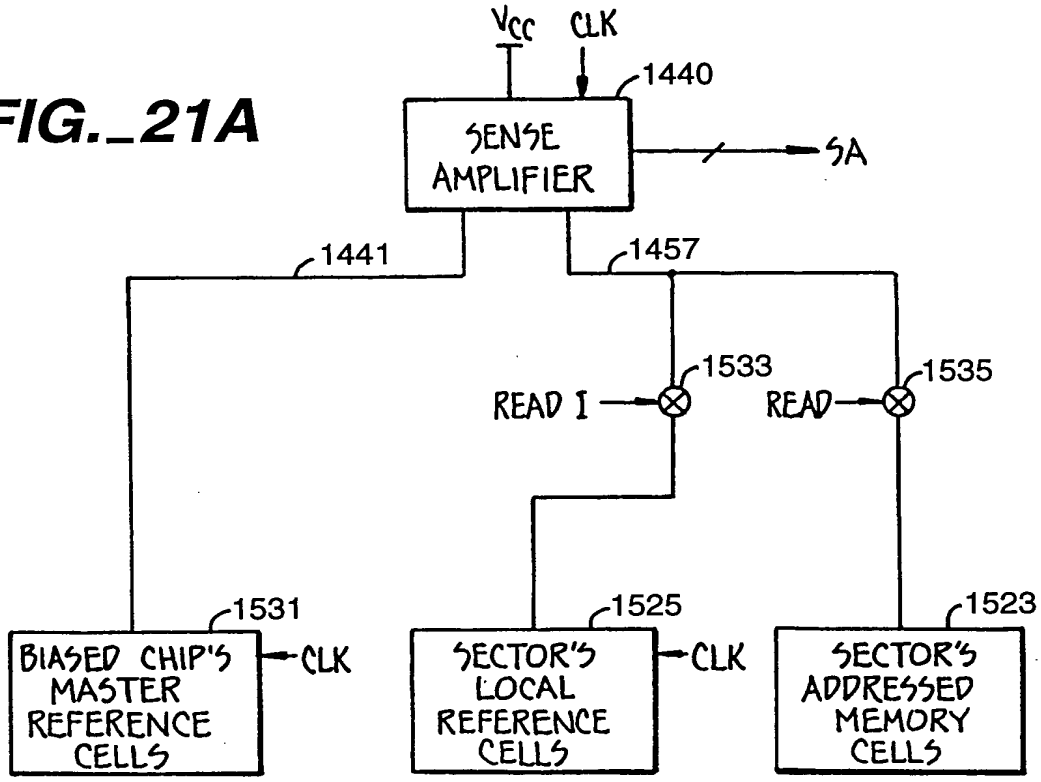


FIG._20B

FIG._21A



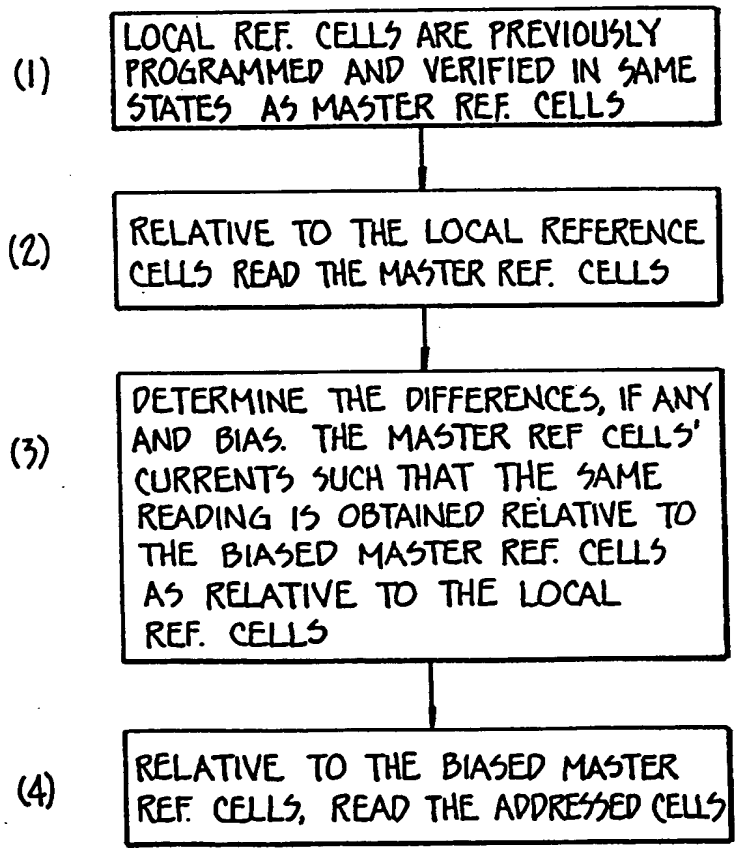


FIG._21D

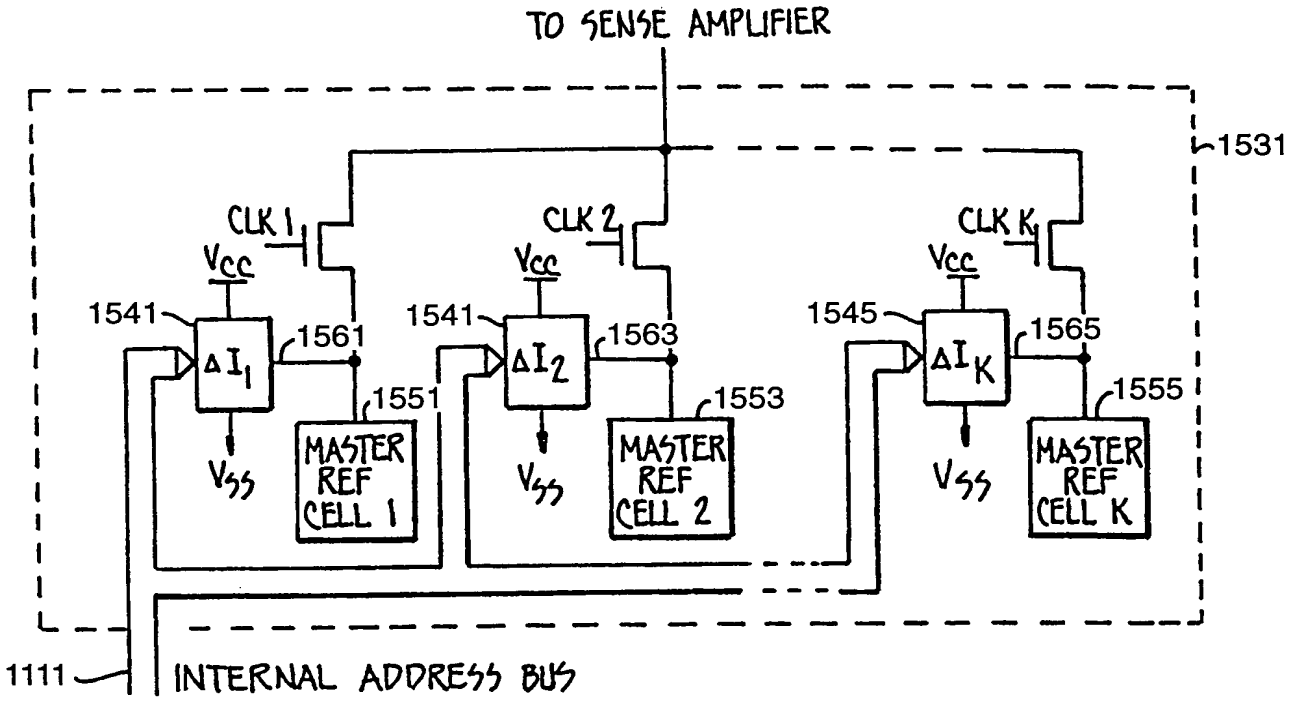


FIG._21B

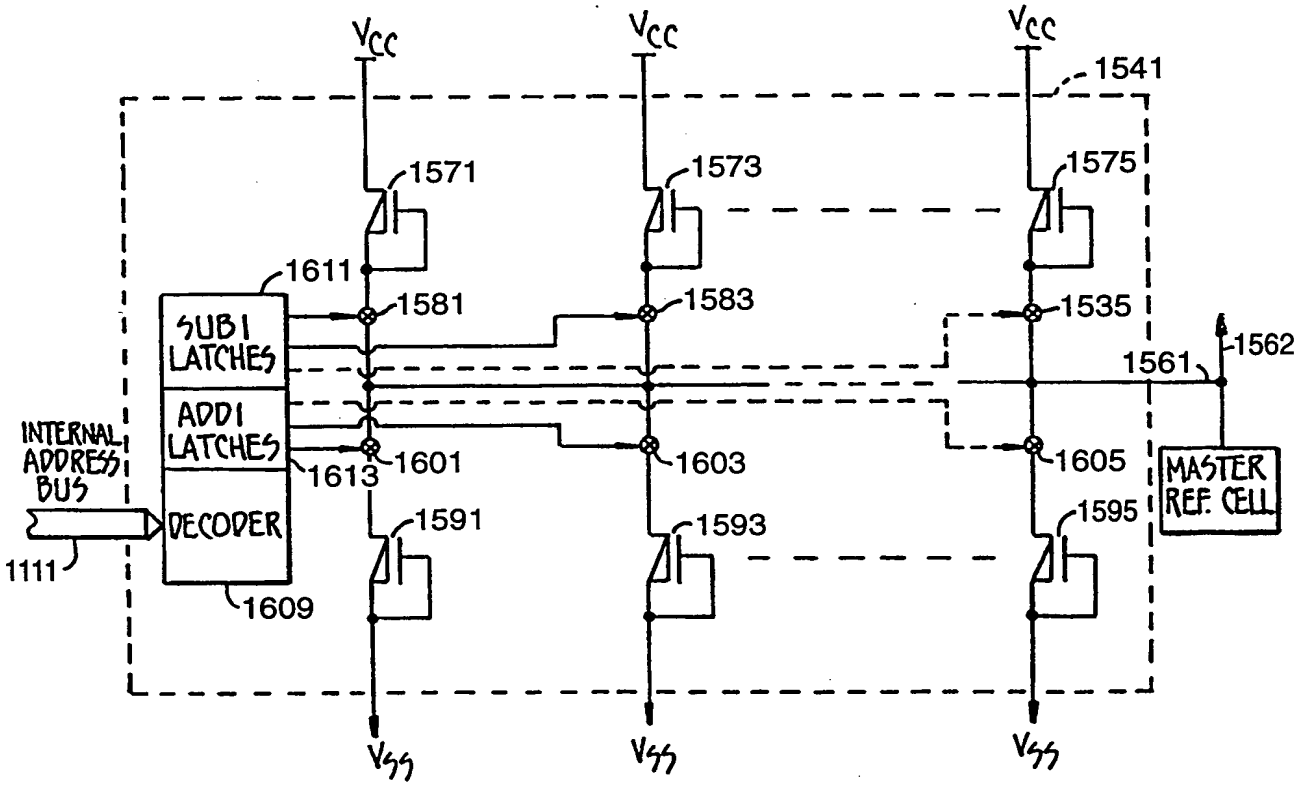
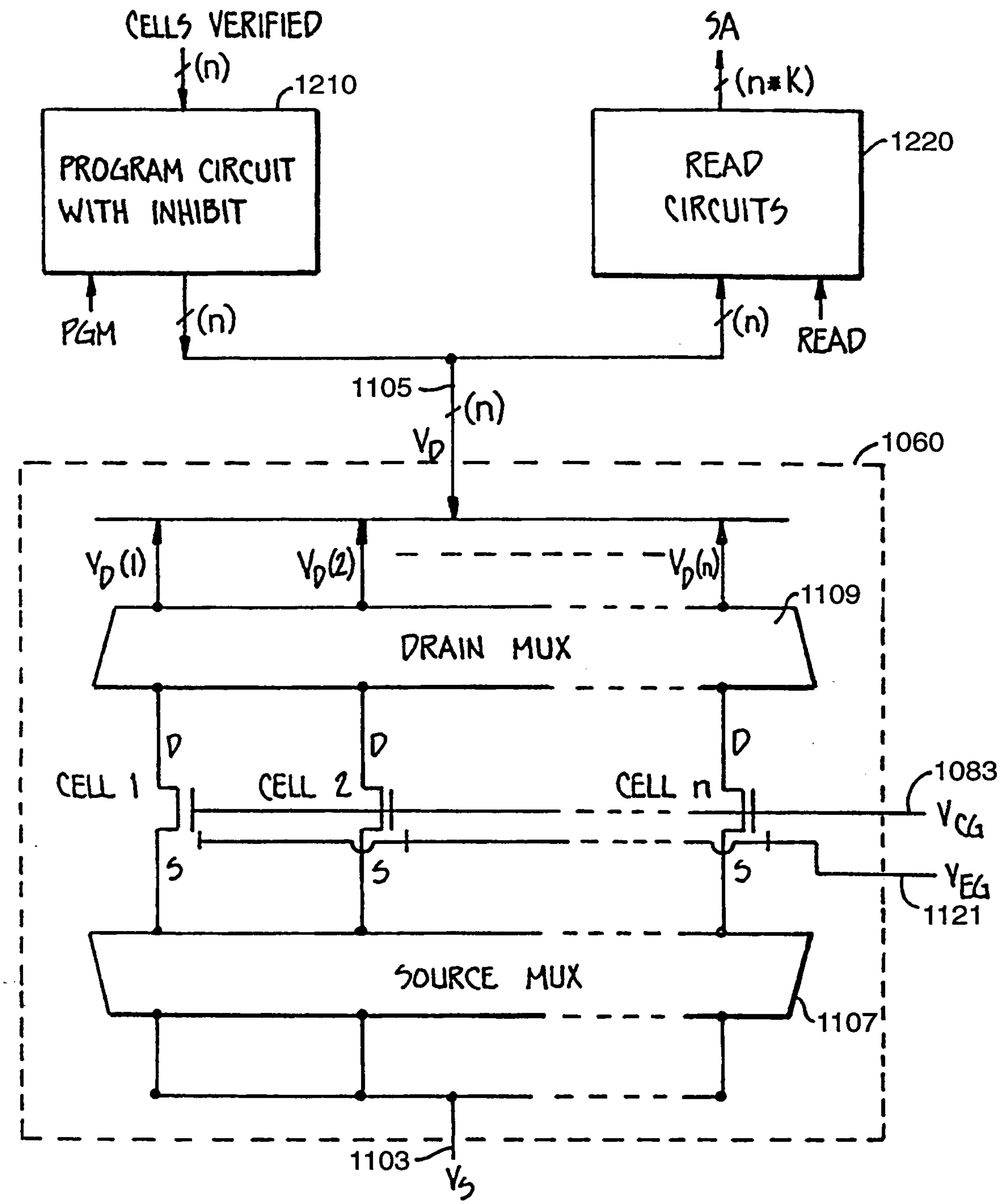
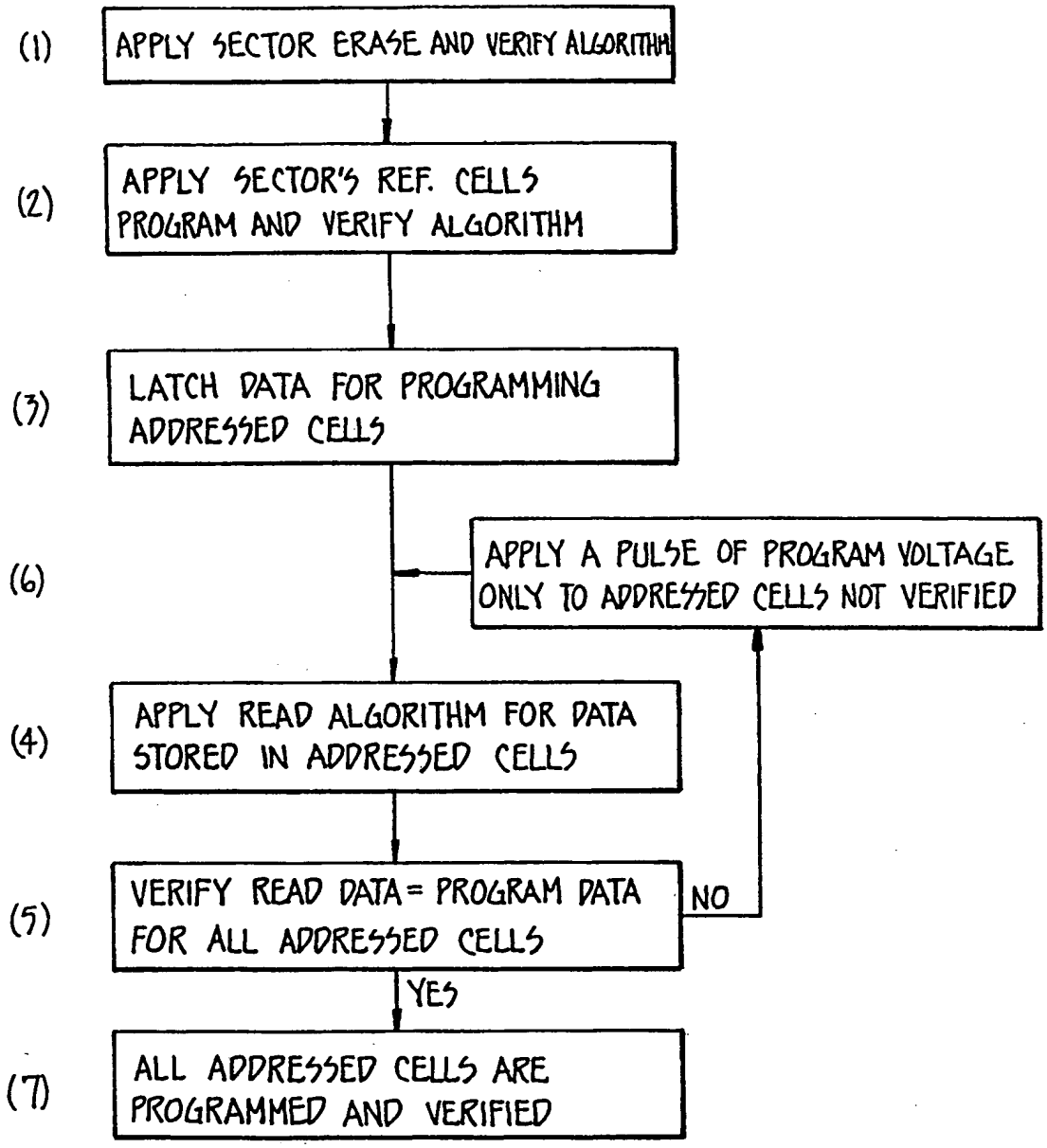


FIG._21C



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG._22



PROGRAM ALGORITHM

FIG._23

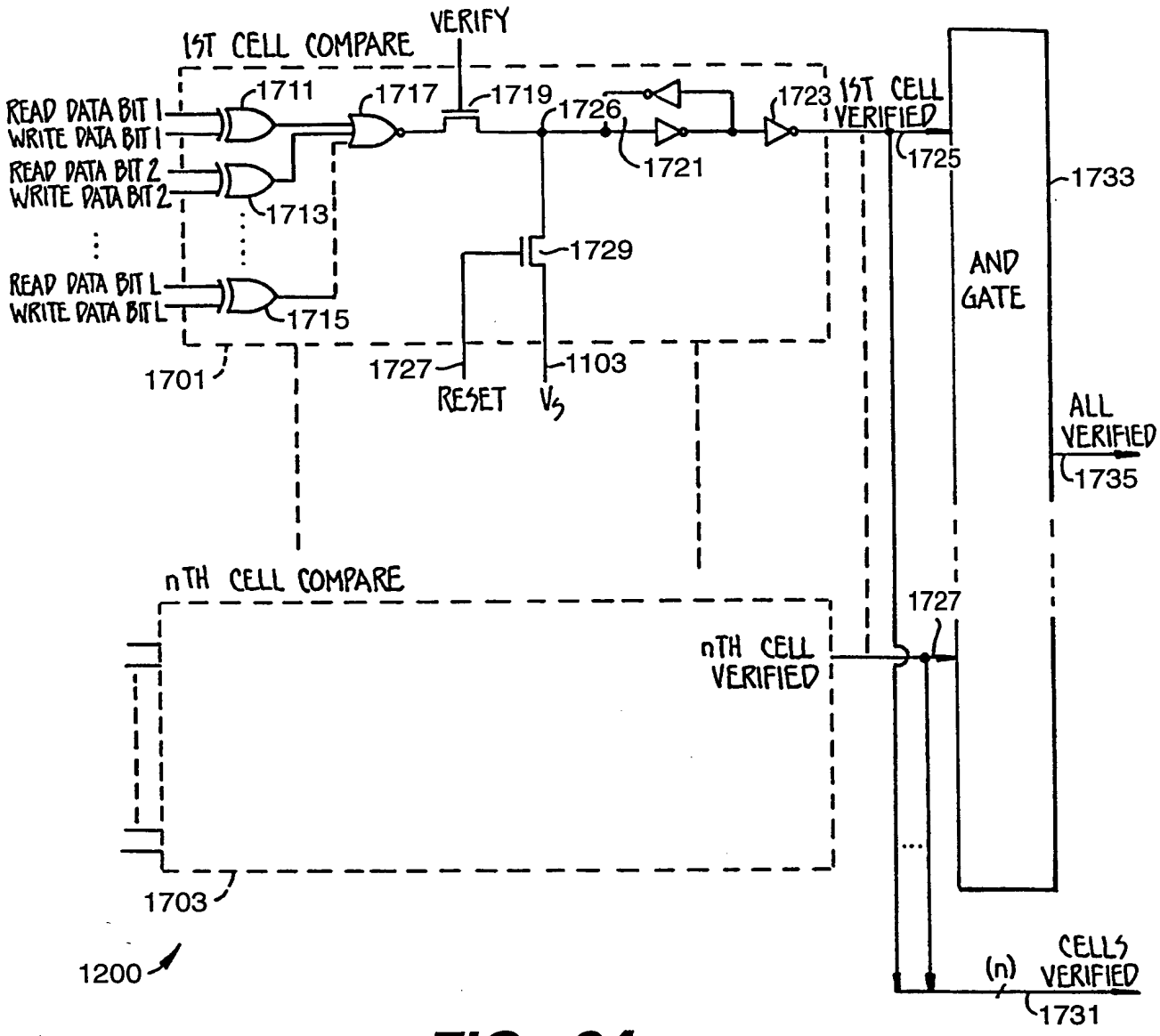

1ST CELL COMPARE
VERIFY
READ DATA BIT 1
WRITE DATA BIT 1
READ DATA BIT 2
WRITE DATA BIT 2
READ DATA BIT L
WRITE DATA BIT L
1711
1717
1719
1726
1723
1721
1725
1733
1713
1729
1715
1701
1727
RESET
1103
1ST CELL VERIFIED
AND GATE
ALL VERIFIED
1735
nTH CELL COMPARE
nTH CELL VERIFIED
1727
1703
1200
(n)
CELLS VERIFIED
1731

FIG._24

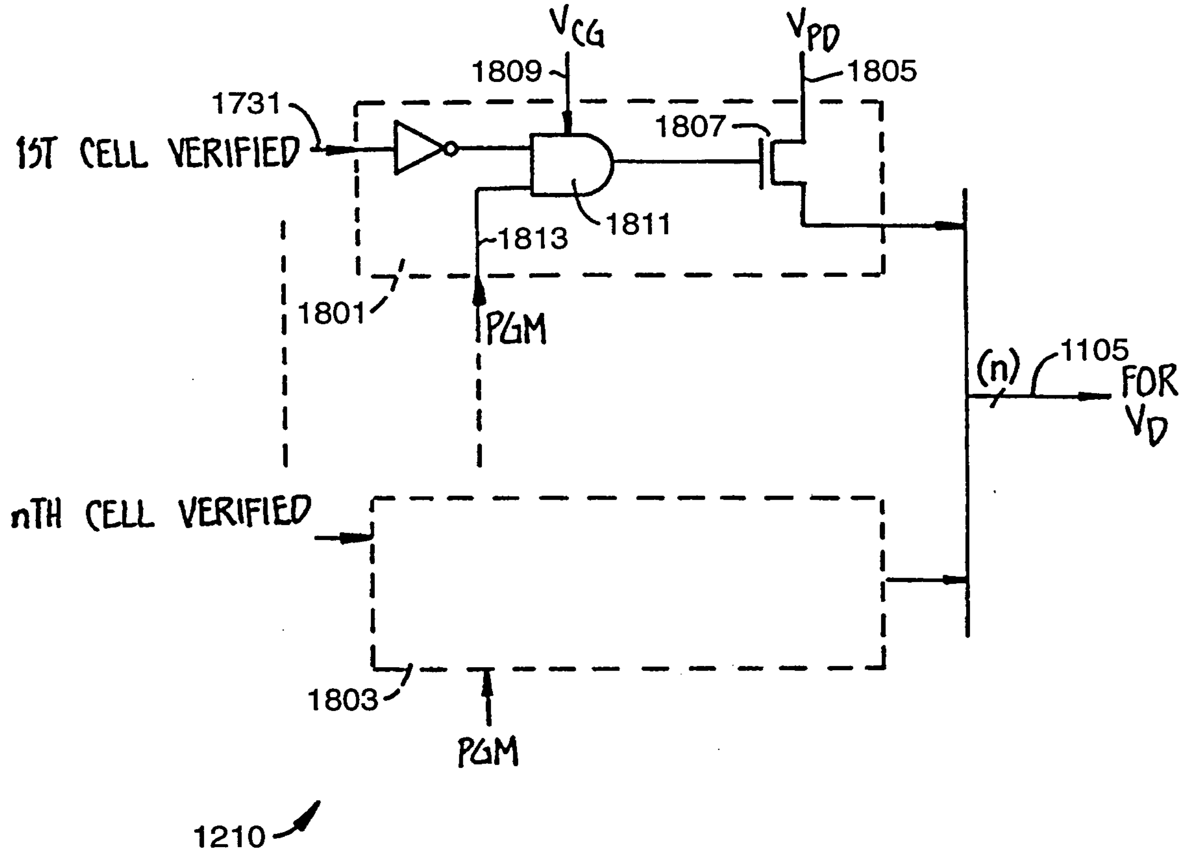


FIG._25

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

TABLE 1

FIG._26

(TYPICAL VALUES)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC}+\delta V$	V_{CC}	$V_{CC}-\delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
UNSELECTED CONTROL GATE	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
UNSELECTED BIT LINE	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

V_{SS}=0V, V_{REF}=1.5V, δV=0.5V - 1V

TABLE 2

FIG._27